# VII. PROPOSED PROCESS FLOWS FOR NMOS PROCESSES

The precautions necessary to make an NMOS process compatible with the low-temperature bonding process have been set forth throughout this report. They are summarized here, as are the two alternative proposed process flows using amorphous silicon or diffused leads. The process flows appear to be quite feasible, and most steps have been carried out successfully. We believe, given the great amount of processing experimentation that we have done to date, that full demonstration of these processes should hold few surprises.

## VII.1 SUMMARY OF PROCESS CONSTRAINTS

Presented in this section are the precautions to observe if bonding at 450°C with the boron-glass process is to be satisfactory.

1. Boron glass should be deposited immediately prior to bonding.
2. The layout should be done so that the bonding will be to thermal $SiO_2$, single-crystal silicon, or smooth, phosphorus-free amorphous silicon.
3. Phosphorus should be excluded fro the process.
4. Any materials containing phosphorus must be capped prior to bonding.
5. Any plasma processing (except for contact holes) must be avoided at the point in the process where there will be no further high-temperature oxidation steps.
6. Photoresist hard-baking must be avoided at the point in the process where there will be no further high-temperature oxidation steps.
7. Aluminum lines must be protected so that cleaning procedures adequate to remove surface residues can be used to return the surface to a cleanliness suitable for bonding.

## VII.2 PROPOSED NMOS PROCESS USING DIFFUSED LEADS

A proposed NMOS process using As diffused leads which observes all the above process constraints is shown in Table VII.1. The process, and the point to which it has been demonstrated, was discussed in Chapter V.10.1.

## VII.3 PROPOSED NMOS PROCESS USING AMORPHOUS SILICON LEADS

A proposed NMOS process using amorphous silicon leads which observes all the above process constraints is shown in Table VII.2. The process, and the point to which it has been demonstrated, was discussed in Chapter V.10.2.

TABLE VII.1 - PROPOSED PROCESS FLOW FOR MOS CAPACITORS WITH DIFFUSED LEADS

0.0 Starting wafers: 18-22 ohm-cm, 4-inch, P-type, <100>.

1.0 Grow pad oxide. Target tox=400 A.
 1.1 TCA clean oxidation tube: STCA5-6.

1.2 Standard clean wafers.
1.3 Pad oxidation: 1 hr 25 minutes, dry $O_2$, SGATEOX, 950°C.
20 minutes $N_2$ anneal.

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2.0 Deposit LPCVD nitride. Target tnit=5000 A.
2.1 Standard clean wafers.
2.2 Deposit $Si_3N_4$: SNITC, 800°C.

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3.0 Pattern for leads implantation.
3.1 Standard clean wafers.
3.2 Dehydrate wafers, 120°C for 10 minutes.
3.3 HMDS: 1.5 minutes.
3.4 Spin photoresist on Eaton; program 10.
3.5 Expose: GCA 6200 10x Wafer Stepper.
3.6 Develop: MTI omnichuck; program 1.
3.7 Descum: Technics-C, $O_2$ plasma, 300 mTorr, 50 watts, 1 minute.
3.8 Hard bake: 20 minutes 120°C in air.

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4.0 Nitride dry etch.
4.1 Chamber clean Technics-C, $O_2$, 300 watts, 15 minutes.
4.2 Plasma etch nitride in Technics-C, $SF_6$/He, 40 watts.

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5.0 Leads implant.
5.1 As, 55 KeV, $5.0 \times 10^{15}/cm^2$.
5.2 Remove photoresist and piranha clean wafers.

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6.0 Oxidation and activation. Target tox=400 A.
6.1 TCA clean oxidation tube: MAIN1-4X.
6.2 Standard clean wafers.
6.3 Oxidize leads area: 1 hr 25 minutes, dry $O_2$, SGATEOX, 950°C.
20 minutes $N_2$ anneal.

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7.0 Pattern for capacitors. <100% aperture opening.
7.1 Standard clean wafers.
7.2 Dehydrate wafers, 120°C for 10 minutes.
7.3 HMDS: 1.5 minutes.
7.4 Spin photoresist on Eaton; program 10.
7.5 Expose: GCA 6200 10x Wafer Stepper.
7.6 Develop: MTI omnichuck; program 1.

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8.0 Nitride dry etch. Front and back!
8.1 Chamber clean Technics-C, $O_2$, 300 watts, 10 minutes.
8.2 Plasma etch nitride in Technics-C, $SF_6$/He, 40 watts.

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9.0 Remove photoresist and clean wafers.

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10.0 Grow field oxide. Target tox=2 µm.
10.1 TCA clean wet oxidation tube: MAIN1-4X.
10.2 Standard clean wafers.
10.3 Field oxidation: SWETOXB, 1000°C.
5 min dry $O_2$
5 hrs wet $O_2$
20 min $N_2$ anneal.

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11.0 Pattern for circuitry recess.
11.1 Standard clean wafers.
11.2 Dehydrate wafers, 120°C for 10 minutes.
11.3 HMDS: 1.5 minutes.
11.4 Spin photoresist on Eaton; program 10.
11.5 Expose: GCA 6200 10x Wafer Stepper.
11.6 Develop: MTI omnichuck; program 1.

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12.0 Oxide wet etch for circuitry recess: 1/5 BHF 6 minutes.

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13.0 Remove photoresist.

14.0 Nitride and pad oxide removal, wet etch.
14.1 Oxide dip: 1:25 HF, 2 minutes.
14.2 Hot phosphoric acid etch (155°C), for >30 minutes.
14.3 Strip off pad oxide 1/10 HF until back side is clear.
Do a 10 second overetch.

15.0 Gate oxidation: Target tox=500 A.
15.1 TCA clean gate oxidation tube: MAIN5-6B.
15.2 Standard clean wafers.
15.3 Gate oxidation: 1 hr, dry $O_2$, SGATEOX, 1000°C.
20 min $N_2$ anneal.

16.0 Phosphorus-free polysilicon deposition: Target tpoly=500 A.
16.1 Immediately after capacitor oxide deposit 500 A of polysilicon: SUPOLY16.

17.0 Pattern for contact holes.
17.1 Standard clean wafers.
17.2 Dehydrate wafers, 120°C for 10 minutes.
17.3 HMDS: 1.5 minutes.
17.4 Spin photoresist on Eaton; program 10.
17.5 Expose: GCA 6200 10x Wafer Stepper.
17.6 Develop: MTI omnichuck; program 1.

18.0 Etch contact holes.
18.1 Plasma etch polysilicon in LAM.
18.2 Plasma etch $SiO_2$ in LAM.
18.3 HF dip.

19.0 Remove photoresist and clean wafers.

20.0 Phosphorus-free polysilicon deposition: Target tpoly=4500 A.
20.1 Standard clean wafers.
20.2 Deposit polysilicon: SUPOLY16.

21.0 Boron-dope polysilicon.
21.1 Best method yet to be determined.
21.2 Activate boron dopant.

22.0 Pattern for capacitor polysilicon.
22.1 Standard clean wafers.
22.2 Dehydrate wafers, 120°C for 10 minutes.
22.2 HMDS: 1.5 minutes.
22.3 Spin photoresist on Eaton; program 10.
22.4 Expose: GCA 6200 10x Wafer Stepper.
22.5 Develop: MTI omnichuck; program 1.

23.0 Polysilicon etch.
23.1 Wet etch polysilicon.
23.2 Remove photoresist and standard clean wafers.

24.0 Deposit LPCVD nitride.
24.1 Standard clean wafers.
24.2 Deposit $Si_3N_4$: SNITC, 800°C.

25.0 Oxidize nitride layer to use in masking.
25.1 Standard clean wafers.
25.2 Wet oxidation: SWETOXB, 1100°C.

26.0 Pattern for nitride capping layer.
26.1 Standard clean wafers.
26.2 Dehydrate wafers, 120°C for 10 minutes.
26.3 HMDS: 1.5 minutes.
26.4 Spin photoresist on Eaton; program 10.

26.5 Expose: GCA 6200 10x Wafer Stepper.
26.6 Develop: MTI omnichuck; program 1.

27.0 Etch oxide: 1/5 BHF.

28.0 Remove photoresist and standard clean wafers. Quick HF dip only!!

29.0 Nitride etch: hot phosphoric acid (155°C-160°C).

30.0 Pattern for leads etchdown.
30.1 Standard clean wafers.
30.2 Dehydrate wafers, 120°C for 10 minutes.
30.3 HMDS: 1.5 minutes.
30.4 Spin photoresist on Eaton; program 10.
30.5 Expose: GCA 6200 10x Wafer Stepper.
30.6 Develop: MTI omnichuck; program 1.

31.0 Oxide wet etch for leads etchdown. Time as needed, 1/5 BHF.

32.0 Remove photoresist and piranha clean wafers.

TABLE VII.2 - PROPOSED PROCESS FLOW FOR MOS CAPACITORS
WITH PHOSPHORUS-FREE AMORPHOUS SILICON LEADS

0.0 Starting wafers: 18-22 ohm-cm, 4-inch, P-type, <100>.

1.0 Grow pad oxide. Target tox=400 A.
1.1 TCA clean oxidation tube: MAIN1-4X.
1.2 Standard clean wafers.
1.3 Pad oxidation: 1 hr 25 minutes, dry $O_2$, SGATEOX, 950°C.
20 minutes $N_2$ anneal.

2.0 Deposit LPCVD nitride. Target tnit=5000A.
2.1 Standard clean wafers.
2.2 Deposit $Si_3N_4$ : SNITC, 800°C.

3.0 Pattern for capacitors. <100% aperture opening.
3.1 Standard clean wafers.
3.2 Dehydrate wafers, 120°C for 10 minutes.
3.3 HMDS: 1.5 minutes.
3.4 Spin photoresist on Eaton; program 10.
3.5 Expose: GCA 6200 10x Wafer Stepper.
3.6 Develop: MTI omnichuck; program 1.

4.0 Nitride etch. Front and back!
4.1 Chamber clean Technics-C, $O_2$, 300 watts, 15 minutes.
4.2 Technics C, $SF_6$/He, 40 watts.

5.0 Remove photoresist.
5.1 MTI omnichuck; program 10.
5.2 Standard clean wafers.

6.0 Grow field oxide. Target tox=2 μm.
6.1 TCA clean wet oxidation tube: MAIN1-4X.
6.2 Standard clean wafers.
6.3 Field oxidation: SWETOXB, 1100°C.
5 minutes dry $O_2$
10 hours wet $O_2$
20 minutes $N_2$ anneal.

7.0 Nitride and pad oxide removal.
7.1 Oxide dip: 3 minutes 1/5 BHF.
7.2 Hot phosphoric acid etch (155°C-160°C ).

8.0 Pattern for circuitry recess.
8.1 Standard clean wafers.
8.2 Dehydrate wafers, 120°C for 10 minutes.
8.3 HMDS: 1.5 minutes.
8.4 Spin photoresist on Eaton; program 10.
8.5 Expose: GCA 6200 10x Wafer Stepper.
8.6 Develop: MTI omnichuck; program 1.

9.0 Oxide etch: 6 minutes 1/5 BHF sink 8.

10.0 Remove photoresist: MTI omnichuck; program 10.

11.0 Pattern for leads recesses.
11.1 Standard clean wafers.
11.2 Dehydrate wafers, 120°C for 10 minutes.
11.3 HMDS: 1.5 minutes.
11.4 Spin photoresist on Eaton; program 10.
11.5 Expose: GCA 6200 10x Wafer Stepper.
11.6 Develop: MTI omnichuck; program 1.

12.0 Oxide etch: 1/5 BHF.

13.0 Remove photoresist and standard clean wafers.

14.0 Gate oxidation: Target tox=500 A.
14.1 TCA clean gate oxidation tube. MAIN5-6B.
14.2 Standard clean wafers.
14.3 Gate oxidation: SGATEOX, 1000°C.
1 hour dry $O_2$
20 minutes $N_2$ anneal.

15.0 Phosphorus-free amorphous silicon deposition: Target t=500 A.
15.1 Immediately after capacitor oxide deposit amorphous silicon: SUPOLY16, 555°C.

16.0 Pattern for contact holes.
16.1 Standard clean wafers.
16.2 Dehydrate wafers, 120°C for 10 minutes.
16.3 HMDS: 1.5 minutes.
16.4 Spin photoresist on Eaton; program 10.
16.5 Expose: GCA 6200 10x Wafer Stepper.
16.6 Develop: MTI omnichuck; program 1.

17.0 Etch contact holes.
17.1 Plasma etch amorphous silicon in LAM.
17.2 Plasma etch $SiO_2$ in LAM.
17.3 HF dip.

18.0 Remove photoresist and clean wafers.

19.0 Phosphorus-free amorphous silicon deposition: Target t dependent on leads recesses.
19.1 Standard clean wafers.
19.2 Deposit amorphous silicon: SUPOLY16, 555°C.

20.0 Boron-dope amorphous silicon.
20.1 Best method yet to be determined.
20.2 Activate boron dopant.

21.0 Pattern for capacitor and leads amorphous silicon.
21.1 Standard clean wafers.
21.2 Dehydrate wafers, 120°C for 10 minutes.
21.3 HMDS: 1.5 minutes.
21.4 Spin photoresist on Eaton; program 10.

21.5 Expose: GCA 6200 10x Wafer Stepper.
21.6 Develop: MTI omnichuck; program 1.

22.0 Amorphous silicon etch.
22.1 Wet etch until all amorphous silicon is removed from back-side of wafer.
22.2 Remove photoresist: MTI omnichuck; program 10.
22.3 Standard clean wafers.